REMARKS

The Office Action mailed February 3, 2006, has been received and reviewed. Claims 1 through 20 were pending in the application. Claims 1 through 9 stand rejected. Claims 10 through 20 were previously withdrawn and are herein canceled, without prejudice, to the filing of one or more divisional applications. Applicant has amended no other claims, and respectfully requests reconsideration of the application as amended herein.

35 U.S.C. § 102(e) Anticipation Rejections

Anticipation Rejection Based on U.S. Patent No. 6,747,465 to Esashi et al.

Claims 1 through 8 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Esashi et al. (U.S. Patent No. 6,747,465). Applicant respectfully traverses this rejection, as hereinafter set forth.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Applicant submits that the Esashi reference does not and cannot anticipate under 35 U.S.C. § 102 the presently claimed invention of independent claim 1, and claims 2-8 depending therefrom, because the Esashi reference does not describe, either expressly or inherently, the identical inventions in as complete detail as are contained in the claims.

The Office Action alleges:

> Esashi teaches the following claimed limitations as cited below:
> 1.(Original) A method for *electrically coupling a first side of a semiconductor substrate to a second side* of said semiconductor substrate, comprising:
> forming a hole having an inner surface from a first side of a semiconductor substrate to a second side of said semiconductor substrate (Fig. 8E (11D)); and
> ***plating*** said inner surface of said semiconductor substrate to form a plated conductive element ***by forcing a plating solution from said first side of said semiconductor substrate to said second side of said semiconductor***

> ***substrate through said hole*** (Fig. 8H (12)). (Office Action, pp. 2-3; emphasis added.)

The Esashi reference discloses no such thing. Furthermore, Applicant respectfully disagrees that the Esashi reference anticipates Applicant's invention as claimed in independent claim 1 which reads:

> 1. A method for electrically coupling a first side of a semiconductor substrate to a second side of said semiconductor substrate, comprising:
> forming a hole having an inner surface from a first side of a semiconductor substrate to a second side of said semiconductor substrate; and
> ***plating*** said inner surface of said semiconductor substrate to form a plated conductive element ***by forcing a plating solution from said first side of said semiconductor substrate to said second side of said semiconductor substrate through said hole.*** (Emphasis added.)

A clear reading of the Esashi reference discloses a plating method that is contrary to Applicant's invention as presently claimed. As stated, Applicant's invention as presently claimed recites, ***"plating ... by forcing a plating solution from said first side of said semiconductor substrate to said second side of said semiconductor substrate through said hole."*** In contrast, the Esashi reference clearly discloses plating performed on a single side since the hole that is to be plated is first sealed closed on the second side thereby prohibiting ***"plating ... by forcing a plating solution from said first side of said semiconductor substrate to said second side of said semiconductor substrate through said hole"*** as claimed by Applicant.

Specifically, the Esashi reference discloses:

> ... As shown in FIG. 8D, by reactive ion etching, the exposed seed layer 11 and the underlying Pyrex glass are removed to ***form a through hole 11D*** having a forward-tapered cross section (such as shown in FIG. 8E). After the nickel-plated layer 11C is removed by an etchant (e.g., aqua regia, etc.) as shown in FIG. 8F, a ***metal plate 11E is applied to the back side of the contactor board 11*** as shown in FIG. 8G. ***This metal plate covers the smaller opening of the through hole 11D.*** By conducting electrolytic ***plating*** using the metal plate 11E as an electrode, ***nickel metal*** is ***buried into the through hole from the right side*** of the contactor board 11 as shown in FIG. 8H, thus forming the conductive member 12. The metal plate 11E is flaked off from the contactor board. (Esashi, col. 8, lines 50-63; emphasis added.)

Not only does the Esashi reference lack disclosure of "plating ... by forcing a plating solution from said first side of said semiconductor substrate to said second side of said semiconductor substrate through said hole", the Esashi reference also lacks disclosure of Applicant's claimed invention of "[a] method for electrically coupling a first side of a semiconductor substrate to a second side of said semiconductor substrate". Specifically in the Esashi reference, once the "nickel metal is buried into the through hole" and "metal plate 11E is flaked off from the contactor board", no electrical connection for "coupling a first side of a semiconductor substrate to a second side of said semiconductor substrate" is possible as electrically conductive plating was prohibited from occurring on the second side. Therefore, the Esashi reference cannot describe Applicant's claimed element of the invention of "[a] method for electrically coupling a first side of a semiconductor substrate to a second side of said semiconductor substrate".

Therefore, independent claim 1, and claims 2-8 depending therefrom, cannot be anticipated by the Esashi reference under 35 U.S.C. § 102. Accordingly, such claims are allowable over the cited prior art and Applicant respectfully requests that such rejections be withdrawn.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on U.S. Patent No. 6,747,465 to Esashi et al.

Claim 9 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Esashi et al. (U.S. Patent No. 6,747,465. Applicant respectfully traverses this rejection, as hereinafter set forth.

> M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:
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> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir.

1991). (Emphasis added).

The nonobviousness of independent claim 1 precludes a rejection of claim 9 which depends therefrom because a dependent claim is obvious only if the independent claim from which it depends is obvious. *See* In re Fine, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988), *see also* MPEP § 2143.03. Therefore, the Applicant requests that the Examiner withdraw the 35 U.S.C. § 102 rejection to independent claim 1 and claim 9 which depends therefrom.

CONCLUSION

Claims 1-9 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicant's undersigned attorney.

Respectfully submitted,

Kevin K. Johanson
Registration No. 38,506
Attorney for Applicant
TRASKBRITT
P.O. Box 2550
Salt Lake City, Utah 84110-2550
Telephone: 801-532-1922

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